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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/083,533	02/27/2002	Hiroshi Hashimoto	020244	6400

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EXAMINER	
LE, THAO X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 09/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/083,533	HASHIMOTO ET AL.	
	Examiner	Art Unit	
	Thao X. Le	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-10 and 12-40* is/are pending in the application.

4a) Of the above claim(s) *16-39* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-10,12-15 and 40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114 was filed in this application after appeal to the Board of Patent Appeals and Interferences, but prior to a decision on the appeal. Since this application is eligible for continued examination under 37 CFR 1.114 and the fee set forth in 37 CFR 1.17(e) has been timely paid, the appeal has been withdrawn pursuant to 37 CFR 1.114 and prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 26 Aug. 2006 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5879990 to Dormans et al. in view of US 6294430 to Fastow et al.

Regarding claims 1, Dormans discloses a semiconductor integrated circuit (IC) device in fig. 9, comprising: a substrate 1, col. 3 line 46, a nonvolatile memory device formed in a memory cell region 4 of substrate 1 and having a multilayer gate electrode 6/10/16/61 structure comprising a tunnel insulating film 6, column 3 line 59, covering substrate 1 and floating gate electrode 10, col. 4 line 10, formed on the tunnel insulating film 6 and having a side wall surfaces covered with a protection insulating film 15 formed of an oxide, col. 4 line 27; a semiconductor device formed in a device region 5 of substrate 1, the semiconductor device comprising a gate insulating film 6 covering substrate 1 and gate electrode 22, formed on the gate insulating film 6; wherein the bird's beak structure (where 15 is located), fig. 2, is formed at an interface of the tunnel insulating film 6 and the floating gate electrode 10, fig. 2, the bird's beak structure penetrating into the floating gate electrode 10 along the interface from the sidewall faces of the floating gate electrode 10, the gate insulating film 6 is interposed between substrate 1and the gate electrode 22 have a uniform thickness at the region under the entire gate electrode 22, fig. 9, wherein the bird's beak structure is a oxide film, column 4 line 27.

But, Dormans does not discloses a semiconductor device wherein the protective insulating film continuously covers sidewall faces and a top surface of

the multilayer gate electrode structure; and wherein the protective insulating film covers the multilayer gate electrode uniformly.

However, Fastow discloses a semiconductor device in fig. 3G comprising a bird's beak (334), a tunnel oxide, a floating gate 308, a ONO dielectric 310, a control gate 312 and a protective insulating film 314/332 continuously covers sidewall faces and a top surface of the multilayer gate electrode structure; and wherein the protective insulating film covers the multilayer gate electrode uniformly. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the protective insulating film 314/332 teaching of Fastow with Dormans's device, because it would have reduces the number of oxides traps in the bird's beak region of the tunnel oxide thus improving the reliability of the floating gate memory device as taught by Fastow in col. 1 lines 10-15.

Regarding claims 2-3, 12, Dormans discloses the IC device wherein the multiplayer gate electrode structure further comprises an insulating film 16, column 4 line 32, formed on the floating gate electrode 10, and a control gate electrode 21, col. 4 line 66, formed on the insulating film 16, wherein each of the gate electrode 22 and control gate electrode 21 comprises doped polysilicon, column 3 line 67 and col. 4 line 54.

Regarding claims 4, 7, 10 and 14, Dormans discloses the IC device wherein the oxide film 15 connects the bird's beak structure, fig. 2, wherein the IC device having the tunnel oxide 6, fig. 2.

Regarding claim 9, Dormans discloses a semiconductor integrated circuit device in fig. 9 comprising: a substrate 1, a nonvolatile memory device formed in a memory cell region 4 of said substrate 1, the nonvolatile memory device comprising: a first active region 11, fig. 9, covered with a tunnel insulating film 6, formed next to the first active region 11 and covered with an insulating film 16, a control gate 21 formed of an embedded diffusion region formed in the first active region; a first gate electrode 10 extending on the tunnel insulating film 6 in the first active region 11 and forming a bridge between the first and second active regions 11/12 to be capacitive-coupled via the insulating film 16 to the embedded diffusion region in the first active region 11, the first gate electrode 10 having sidewall faces thereof covered with a protection insulating film 15 formed of a oxide film; and a diffusion region formed on each of sides of the first gate electrode10 in the first active region; and a semiconductor device formed in a device region 5 of substrate 1, the semiconductor device comprising a gate insulating film 6 covering substrate 1 and a second gate electrode 22 formed on the gate insulating film 6, fig. 9, wherein a bird's beak structure (wherein 15 is located) is formed of oxide film at an interface of the tunnel insulating film 6 and the first gate electrode 10, the bird's beak structure penetrating into the first gate electrode 10 along the interface of the first gate electrode 10; the gate insulating film 6 is interposed between said substrate 1 and the second gate electrode 22 to have a uniform thickness at the region under the entire gate electrode 22, fig. 9, wherein the bird's beak structure is a oxide film.

But, Dormans does not discloses a semiconductor device comprising a second active region formed next to the first active region and wherein the

protective insulating film continuously covers sidewall faces and a top surface of the multilayer gate electrode structure; and wherein the protective insulating film covers the multilayer gate electrode uniformly.

However, Fastow discloses a semiconductor device in fig. 3G comprising a first active region n and n+ (double diffused regions), fig. 1 and fig. 3G, a bird's beak (334), a tunnel oxide, a floating gate 308, a ONO dielectric 310, a control gate 312 and a protective insulating film 314/332 continuously covers sidewall faces and a top surface of the multilayer gate electrode structure; and wherein the protective insulating film covers the multilayer gate electrode uniformly. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the double diffused regions and protective insulating film 314/332 teaching of Fastow with Dormans's device, because it would have created an EEPROM device reducing the number of oxides traps in the bird's beak region of the tunnel oxide thus improving the reliability of the floating gate memory device as taught by Fastow in col. 1 lines 10-15.

Regarding claim 40, as discussed in the above claims 1-4, and 12, the combination of Dormans and Fastow disclose all the limitations of claim 40.

5. Claims 6, 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5879990 to Dormans et al. and US 6294430 to Fastow et al. as applied to claims 1 and 9 above and further in view of US 6406959 to Prall et all.

Regarding claims 6, 13, Dormans does not expressly disclose the semiconductor IC device wherein a SOI substrate is employed as substrate.

However, Prall reference discloses a flash memory device wherein the substrate 11 can be either silicon or SOI, column 4 line 15. At the time of the invention was made; it would have been obvious to one of ordinary skill in the art to replace the silicon substrate of Dormans with either Si or SOI substrate teaching of Prall, because such substrate substitution would have been considered a mere substitution of art-recognized equivalent values.

6. Claims 8 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over 5879990 to Dormans et al and US 6294430 to Fastow et al. as applied to claims 1 and 9 above and further in view of Applicant Admitted Prior Art (APA)

Regarding to claims 8 and 15, Dormans does not discloses the tunnel insulating film is a nitride oxide film.

However, APA discloses the IC device having the tunnel oxide 12, spec. page 2 or nitride, page 4. At the time of the invention was made; it would have been obvious to one of ordinary skill in the art to use the tunnel insulating material teaching of APA in the Dormans's device, because such material substitution would have been considered a mere substitution of art-recognized equivalent values.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

20 Sept. 2006

THAO X. LE
PRIMARY PATENT EXAMINER